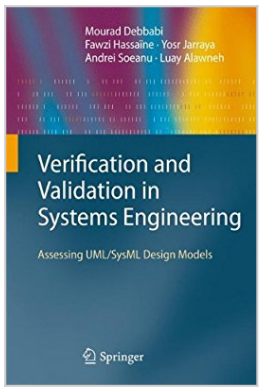

Verification and Validation in Systems Engineering: Assessing UML/SysML Design Models

By Mourad Debbabi, Fawzi Hassaïne, Yosr Jarraya, Andrei Soeanu, Luay Alawneh

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At the dawn of the 21st century and the information age, communication and c- puting power are becoming ever increasingly available, virtually pervading almost every aspect of modern socio-economical interactions. Consequently, the potential for realizing a signi?cantly greater number of technology-mediated activities has emerged. Indeed, many of our modern activity ?elds are heavily dependant upon various underlying systems and software-intensive platforms. Such technologies are commonly used in everyday activities such as commuting, traf?c control and m- agement, mobile computing, navigation, mobile communication. Thus, the correct function of the forenamed computing systems becomes a major concern. This is all the more important since, in spite of the numerous updates, patches and ?rmware revisions being constantly issued, newly discovered logical bugs in a wide range of modern software platforms (e. g. , operating systems) and software-intensive systems (e. g. , embedded systems) are just as frequently being reported. In addition, many of today’s products and services are presently being deployed in a highly competitive environment wherein a product or service is succeeding in most of the cases thanks to its quality to price ratio for a given set of features. Accordingly, a number of critical aspects have to be considered, such as the ab- ity to pack as many features as needed in a given product or service while c- currently maintaining high quality, reasonable price, and short time -to- market.

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Editorial Review

Review

From the reviews:

“The five authors of this book tackle a very difficult subject, and must be commended for doing so. The result is a welcome addition to the body of professional literature. … It is a highly technical … book on one of the most critical subjects that we have, as professionals. … The book is exceedingly well illustrated. … a professional involved in systems engineering, and particularly in systems quality, verification, systems verification, or other related activities, would find this book useful.” (Mordechai Ben-Menachem, ACM Computing Reviews, May, 2011)

From the Back Cover

Verification and validation represents an important process used for the quality assessment of engineered systems and their compliance with the requirements established at the beginning of or during the development cycle.

Debbabi and his coauthors investigate methodologies and techniques that can be employed for the automatic verification and validation of systems engineering design models expressed in standardized modeling languages. Their presentation includes a bird’s eye view of the most prominent modeling languages for software and systems engineering, namely the Unified Modeling Language (UML) and the more recent Systems Modeling Language (SysML). Moreover, it elaborates on a number of quantitative and qualitative techniques that synergistically combine automatic verification techniques, program analysis, and software engineering quantitative methods applicable to design models described in these modeling languages. Each of these techniques is additionally explained using a case study highlighting the process, its results, and resulting changes in the system design.

Researchers in academia and industry as well as students specializing in software and systems engineering will find here an overview of state-of-the-art validation and verification techniques. Due to their close association with the UML standard, the presented approaches are also applicable to industrial software development.

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